

Serial No. 09/844,347

Filing Date: April 27, 2001

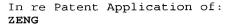
Independent Claims 32 and 36 already recite that the source/body contact regions "non-interruptibly contact the source regions." Consequently, no new issues are being raised by this amendment.

Independent Claim 32 has also been amended to correct a noted informality. Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached paper is captioned "Version with Markings to Show Changes Made." The arguments supporting patentability of the claim amendment and the claims are presented in detail below.

I. Independent Claims 23 and 36 Are Patentable

The Examiner rejected independent Claims 23 and 36 over the Applicant's prior art FIGS. 1 and 3a-3b in view of the Beasom patent. The Applicant's prior art figures are directed to a conventional trench-gated power MOSFET. Beasom is directed to an insulated gate MOSFET having a minority carrier diode and a majority carrier diode formed in the drain region.

The present invention, as recited in independent Claim 23, for example, is directed to a MOSFET comprising a semiconductor layer having a trench therein, a gate dielectric layer lining the trench, and a gate conducting layer in a lower portion of the trench. A dielectric layer is in an upper portion of the trench and extends outwardly from the semiconductor layer. The MOSFET further includes source regions adjacent the outwardly extending dielectric layer, and source/body contact regions laterally spaced apart from the gate conducting layer and non-interruptibly contacting the source regions.



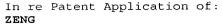
Serial No. 09/844,347 Filing Date: April 27, 2001

The MOSFET is advantageously formed with a reduced on-resistance without degrading device ruggedness. The on-resistance is reduced since each MOSFET includes a source/body contact region that is laterally spaced apart from the gate conducting layer and non-interruptibly contacts the source regions. The source/body contact regions thus provide an efficient short between the source and body regions of the MOSFET. As a result, device ruggedness is increased.

Referring now more particularly to the Applicant's prior art FIGS. 1 and 3a-3b, the Examiner correctly notes that the source/body contact regions 18 in the illustrated MOSFET are not laterally spaced apart from the gate conducting layer 12 as recited in the claimed invention. The Examiner cited the Beasom patent as disclosing this feature.

Referring in particular to FIG. 2 in Beasom, the illustrated transistor includes a body region 12, a source region 14 and a gate conducting layer 16. The Examiner has characterized contact region 20 as the source/body contact region. However, amended independent Claim 23 recites that the source/body contact regions non-interruptibly contact the source regions. In sharp contrast, contact region 20 in Beasom is spaced apart from the source region 14. In other words, the contact region 20 is not in contact with the source region 14. Consequently, Beasom refers to contact region 20 as a body contact region (column 3, line 25) instead of a source/body contact region.

Even if the references were combined as suggested by the Examiner, the claimed invention is still not produced. That is, the Applicant's prior art figures and the Beasom patent fail to teach or suggest that the source/body contact



Serial No. 09/844,347

Filing Date: April 27, 2001

regions non-interruptibly contact the source regions of the MOSFET.

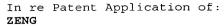
Accordingly, it is submitted that independent Claim 23 is patentable over the Applicant's prior art FIGS. 1 and 3a-3b in view of the Beasom patent. Independent Claim 36 is similar to independent Claim 23. Accordingly, it is also submitted that independent Claim 36 is patentable over the Applicant's prior art FIGS. 1 and 3a-3b in view of the Beasom patent.

II. Independent Claim 32 Is Patentable

The Examiner rejected independent Claim 32 over the Applicant's prior art FIGS. 1 and 3a-3b in view of the Beasom patent and in further view of the Gilbert et al. patent. The Applicant's prior art figures and Gilbert et al. are directed to trench-gated power MOSFETS. Beasom is directed to an insulated gate MOSFET having a minority carrier diode and a majority carrier diode formed in the drain region.

Independent Claim 32 is similar to amended independent Claim 23 but further recites a source electrode on the source regions and on the dielectric layer, and at least one conductive via between the source electrode and the source/body contact regions.

The deficiencies of the prior art FIGS. 1 and 3a-3b and the Beasom patent have been discussed in detail above. That is, these references fail to teach or suggest that the source/body contact regions non-interruptibly contact the source regions of the MOSFET. It is respectfully submitted that the Gilbert et al. patent fails to provide this noted deficiency. As correctly noted by the Examiner, the combination of these two references also fails to disclose at



Serial No. 09/844,347

Filing Date: April 27, 2001

least one conductive via between the source electrode and the source/body contact regions as recited in independent Claim 32. The Examiner cited Gilbert et al. as disclosing this feature.

Referring now to the Gilbert et al. patent, and in particular FIG. 5F, the Examiner has characterized a conductive via extending between a source electrode 90 and a source/body contact region 64. Applicant respectfully asserts that the conductive via actually extends between the source electrode 90 and the N+ source region. The N+ source region is adjacent the source/body contact region 64. This is in sharp contrast to the claimed invention wherein the at least one conductive via extends between the source electrode and the source/body contact regions.

Even if the references were combined as suggested by the Examiner, the claimed invention is still not produced. That is, the Applicant's prior art figures in view of the Beasom patent and in further view of the Gilbert et al. patent fail to teach or suggest that the source/body contact regions non-interruptibly contact the source regions of the MOSFET, and that the at least one conductive via extends between the source electrode and the source/body contact regions.

Accordingly, it is submitted that independent Claim 36 is patentable over the Applicant's prior art FIGS. 1 and 3a-3b in view of the Beasom patent and in further view of the Gilbert et al. patent. In view of the patentability of independent Claims 23, 32 and 36, it is submitted that their dependent claims which recite yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

Serial No. 09/844,347

Filing Date: April 27, 2001

CONCLUSION

In view of the claim amendments and arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

Michael W. Taylor

Reg. No. 43,182

Allen, Dyer, Doppelt, Milbrath

& Gilchrist, P.A.

255 S. Orange Avenue, Suite 1401 Post Office Box 3791

Orlando, Florida 32802

407/841-2330

Serial No. 09/844,347

Filing Date: April 27, 2001

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

The claims have been amended as follows:

23. (Twice Amended) A MOSFET comprising:

a semiconductor layer having a trench therein;

a gate conducting layer in a lower portion of the trench;

a dielectric layer in an upper portion of the trench and extending outwardly from said semiconductor layer;

source regions adjacent the outwardly extending dielectric layer; and

source/body contact regions laterally spaced apart from said gate conducting layer and non-interruptibly contacting said source regions.

- 31. (Amended) A MOSFET comprising:
- a semiconductor layer having a trench therein;
- a gate dielectric layer lining the trench;
- a gate conducting layer in a lower portion of the trench;

a dielectric layer in an upper portion of the trench and extending outwardly from said semiconductor layer;

source regions adjacent the outwardly extending dielectric layer;

source/body contact regions laterally spaced from said gate conducting layer and non-interruptibly contacting said source regions;

a source electrode on said source regions and on said dielectric layer; and

Serial No. 09/844,347

Filing Date: April 27, 2001

at least one conductive via between said source electrode and said source/body contact regions[; and a source electrode on said source regions, on said dielectric layer and on said at least conductive via].

Serial No. 09/844,347

Filing Date: April 27, 2001



CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: DIRECTOR, U.S. PATENT AND TRADEMARK OFFICE, WASHINGTON, D.C. 20231, on this day of November, 2002.

twin & Gelian

NUV 15 2002 TC 2800 MAIL ROOM